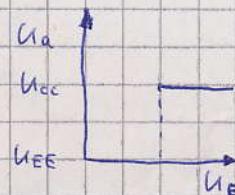
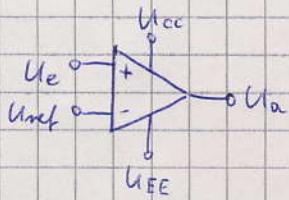


Komparatoren

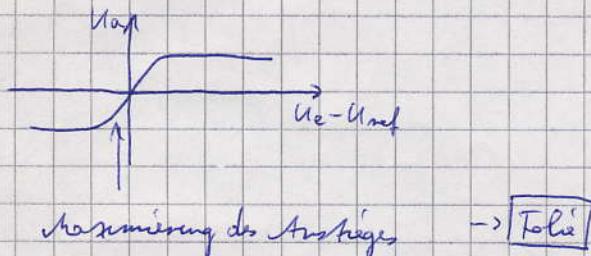


Realisierung ähnlich OPV, aber andere Zieldaten

- hohe Verstärkung
- geringer Offset
- sehr hohe slew rate
- keine Gegenkopplung \rightarrow Stabilität unzuverlässig

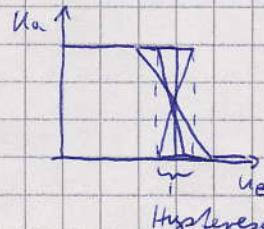
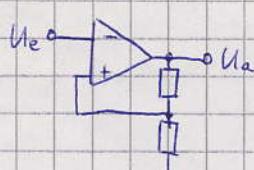
\rightarrow Tolle ADC MP580

Ausgangspunkt: Differenzstufe



Möglichkeiten:

- Erhöhung von g_m
- Erhöhung der R_c
- \Rightarrow mitkopplung



\rightarrow [Tolle] Hysterese

Problem: - kein U_{ref} -Eingang vorhanden,
 U_{ref} wird durch Schaltungsdimensionierung bestimmt

- \hookrightarrow Erweiterung der Schaltung, gestaltete Komparator
- \hookrightarrow [Tolle] galvanische Komparator

Phase 1) $U_x > 0$, normaler Differenzverstärker arbeitet, $U_o = v(U_e - U_{ref})$

Phase 2) $U_o(0) = th_{av}(U_e - U_{ref})$

- mitgekoppelte Struktur aktiv
- Differenzverstärker deaktiviert

FEATURES

- 150 ps propagation delay
- 25 ps overdrive and slew rate dispersion
- 8 GHz equivalent input rise time bandwidth
- 100 ps minimum pulse width
- 35 ps typical output rise/fall
- 10 ps deterministic jitter(DJ)
- 200 fs random jitter (RJ)
- 2 V to +3 V input range with +5 V/-5.2 V supplies
- On-chip terminations at both input pins!
- Resistor-programmable hysteresis
- Differential latch control
- Power supply rejection > 70 dB

APPLICATIONS

- Automatic test equipment (ATE)
- High speed instrumentation
- Pulse spectroscopy
- Medical imaging and diagnostics
- High speed line receivers
- Threshold detection
- Peak and zero-crossing detectors
- High speed trigger circuitry
- Clock and data signal restoration

GENERAL DESCRIPTION

The ADCMP580/ADCMP581/ADCMP582 are ultrafast voltage comparators fabricated on Analog Devices, Inc.'s proprietary XFCB3 Silicon Germanium (SiGe) bipolar process. The ADCMP580 features CML output drivers; the ADCMP581 features reduced swing ECL (negative ECL) output drivers; and the ADCMP582 features reduced-swing PECL (positive ECL) output drivers.

The three comparators offer 150 ps propagation delay and 100 ps minimum pulse width for 10 Gbps operation with 200 fs random jitter (RJ). Overdrive and slew rate dispersion is typically less than 25 ps.

FUNCTIONAL BLOCK DIAGRAM

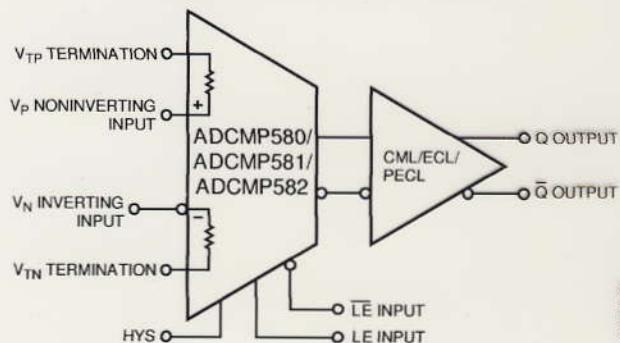


Figure 1.

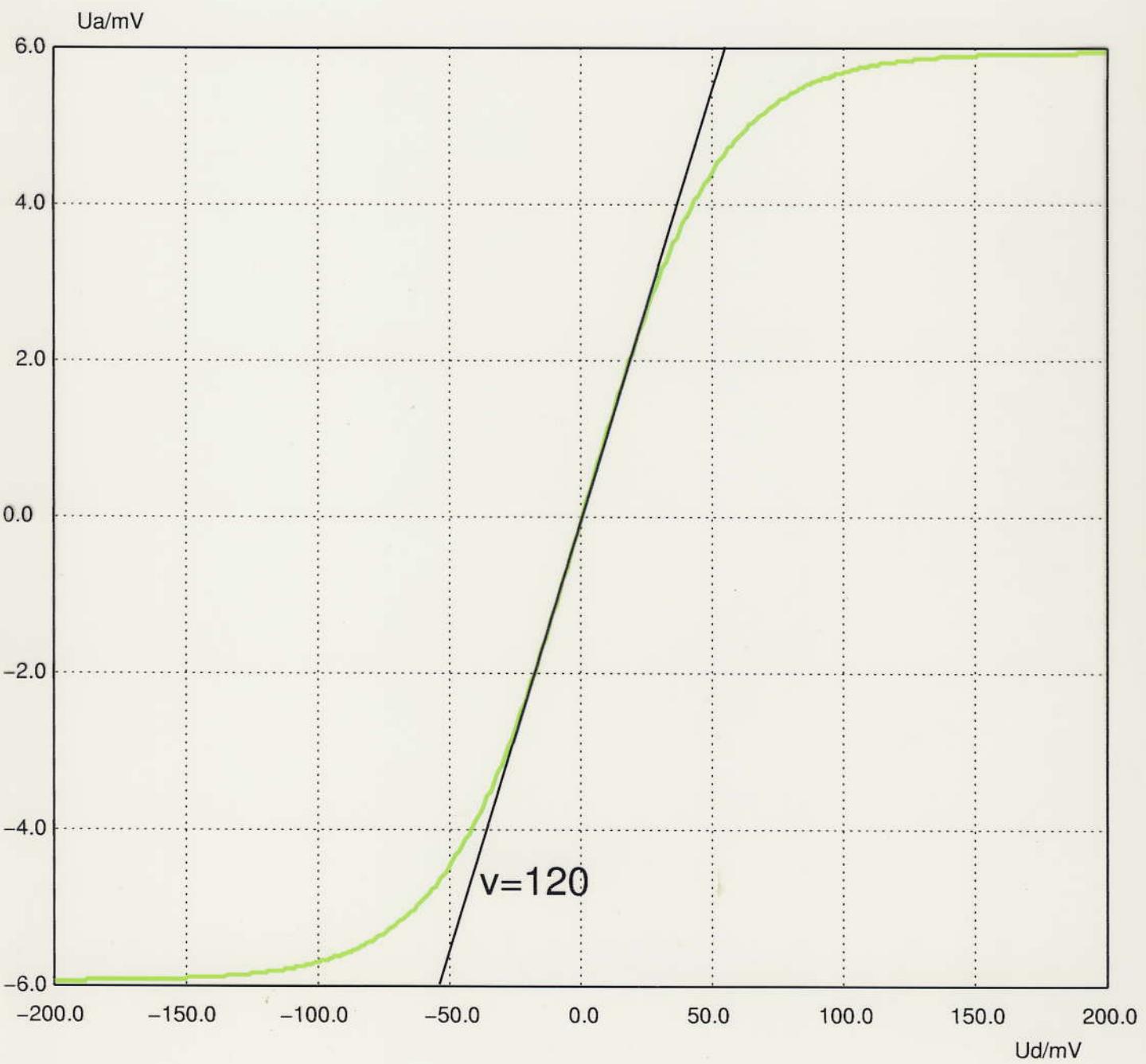
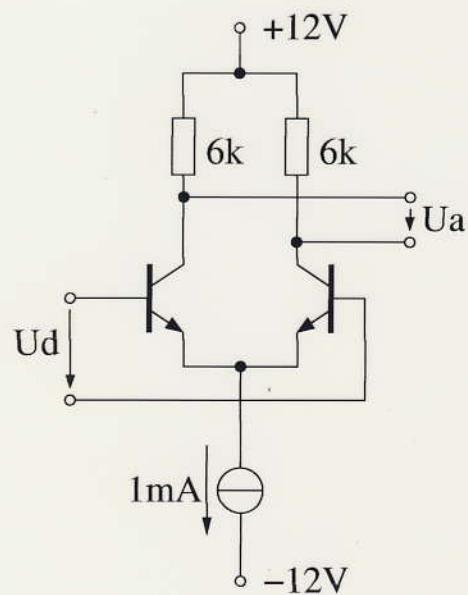
The ±5 V power supplies enable a wide -2 V to +3 V input range with logic levels referenced to the CML/NECL/PECL outputs. The three inputs have 50 Ω on-chip termination resistors with the optional capability to be left open (on an individual pin basis) for applications requiring high impedance input.

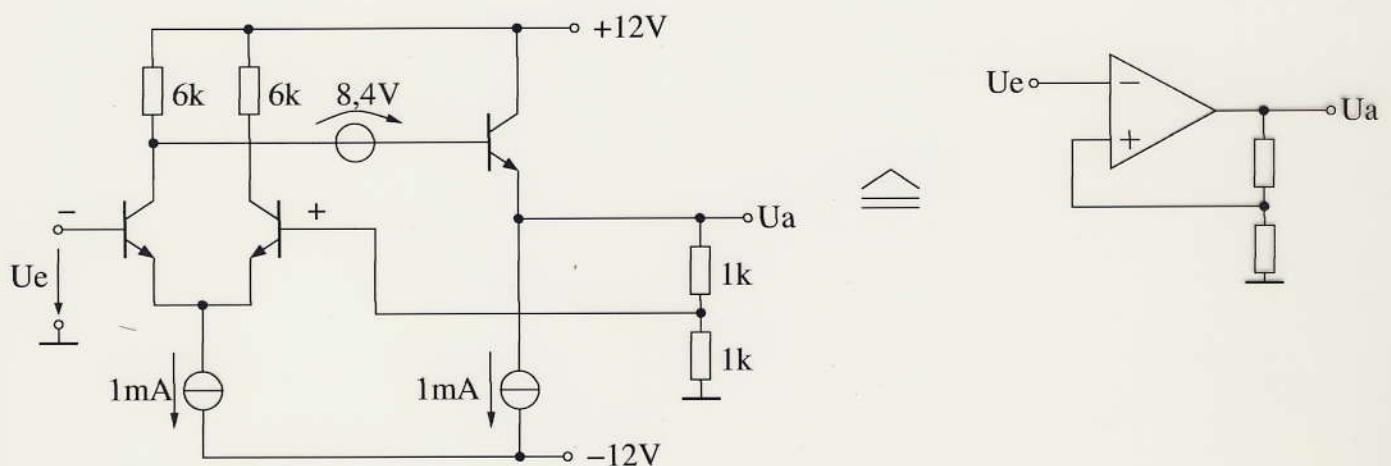
The CML output stage is designed to directly drive 400 mV into 50 Ω transmission lines terminated to ground. The NECL output stages are designed to directly drive 400 mV into 50 Ω terminated to -2 V. The PECL output stages are designed to directly drive 400 mV into 50 Ω terminated to $V_{CCO} - 2$ V. High speed latch and programmable hysteresis are also provided. The differential latch input controls are also 50 Ω terminated to an independent V_{TT} pin to interface to either CML or ECL or to PECL logic.

The ADCMP580/ADCMP581/ADCMP582 are available in a 16-lead LFCSP package.

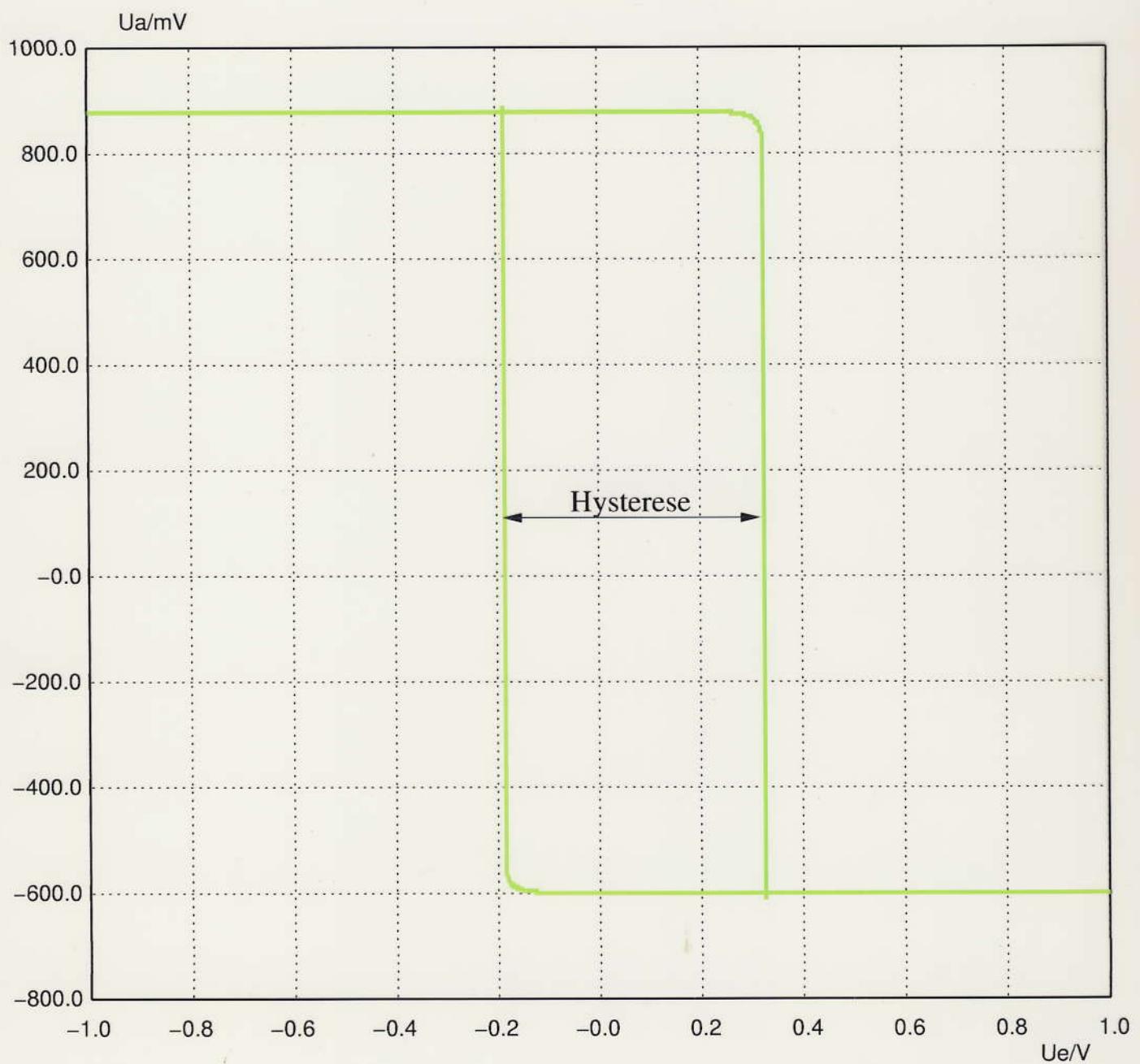
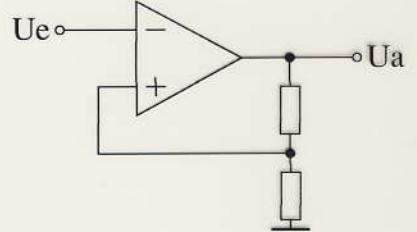
Rev. PrA

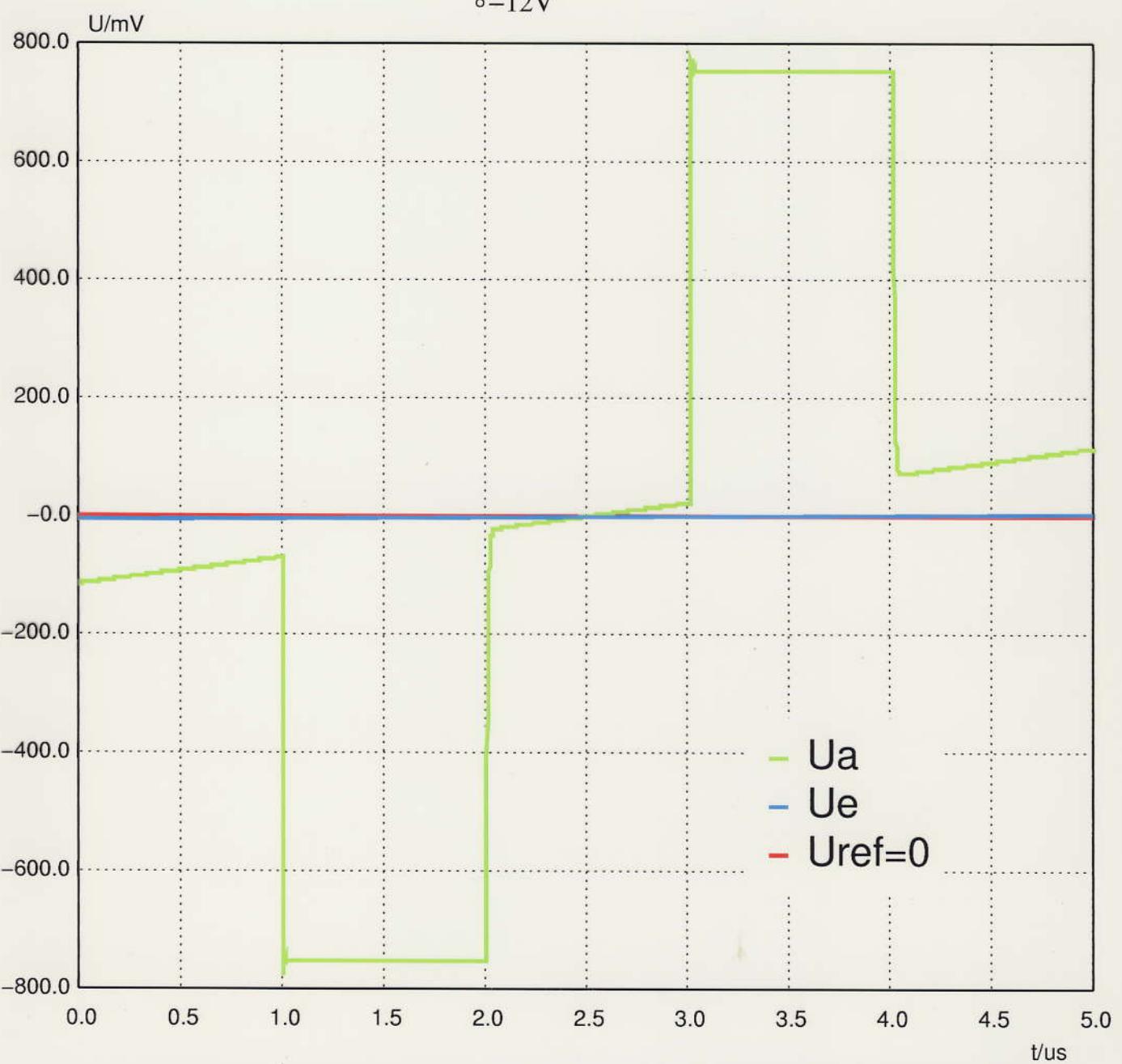
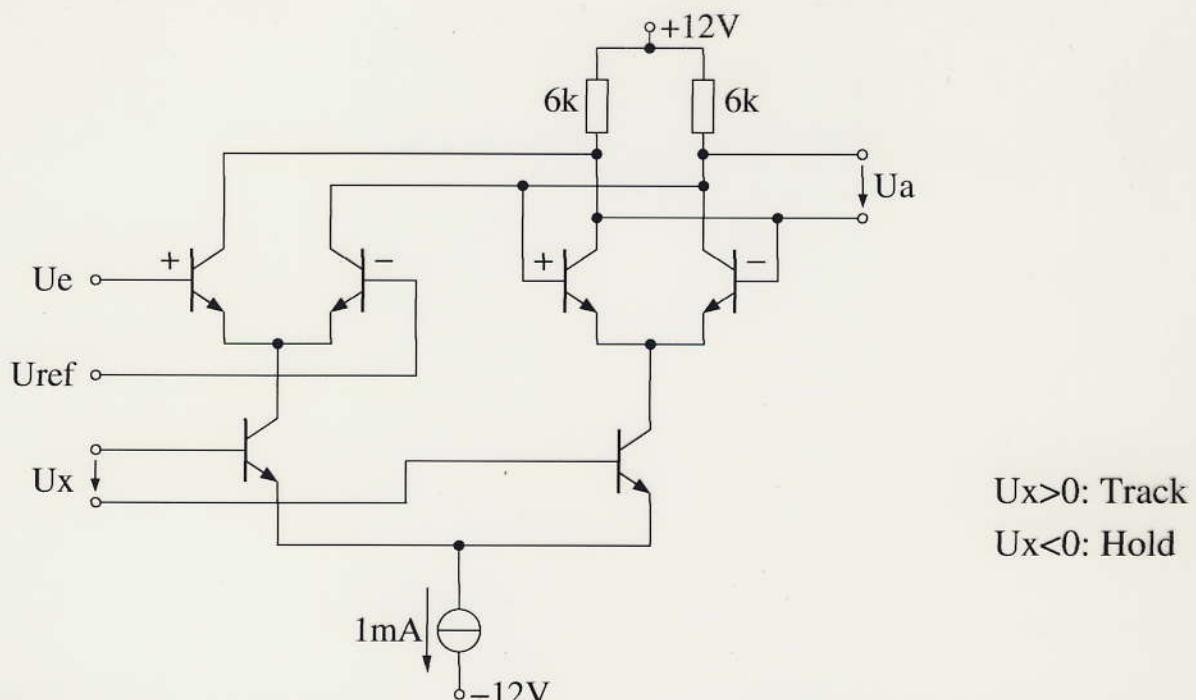
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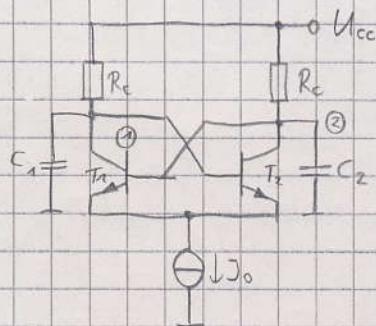
\triangle





Track	Hold	Track	Hold	Track
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mitkopplung:



Kleinsignalverhalten:

$$\begin{aligned} M_1 (c_1) &= g_m M_2 \quad (1) \\ r_{BE1} \| R_{b1} \| r_{BE2} \| R_{b2} \| r_{DE1} & \quad (2) \\ g_m M_1 = c_2 & \quad (3) M_2 \end{aligned}$$

$$r_{BE} \| R_c = R$$

$$(1) \quad g_m M_2 + \frac{M_1}{R} + c_1 i_{in} = 0$$

$$(2) \quad g_m M_1 + \frac{M_2}{R} + c_2 i_{in} = 0$$

$$M_a = M_1 - M_2 \quad ; \quad C_1 = C_2 = C$$

$$\rightarrow (R g_m + (1 - g_m R)) u_{in} = 0$$

$$M_a(t) = U_a(0) e^{at} \quad a = \frac{g_m R - 1}{R \cdot C}$$

$$\begin{cases} \downarrow \\ g_m R \leq 1 \\ \rightarrow U_a \rightarrow 0 \end{cases}$$

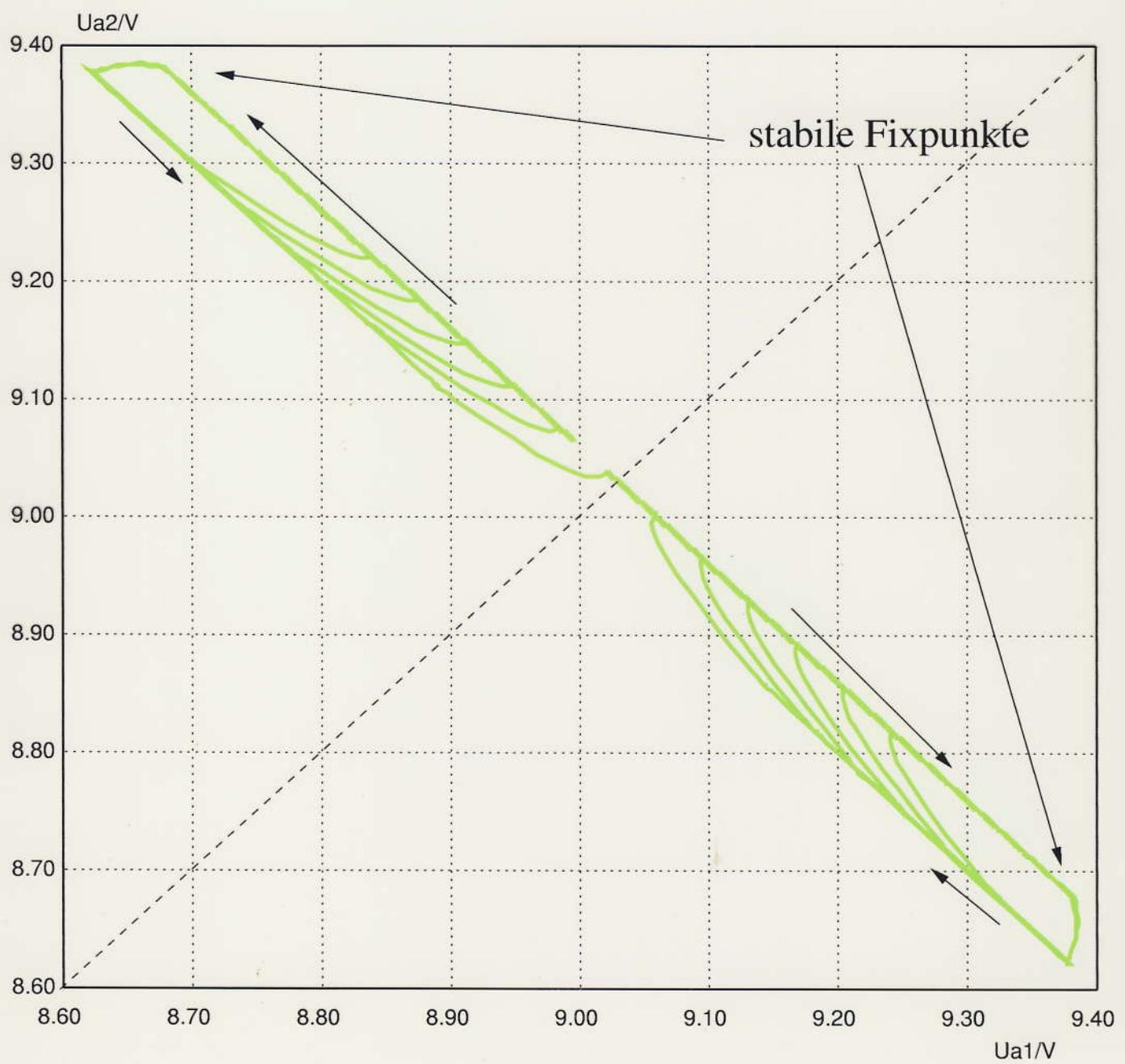
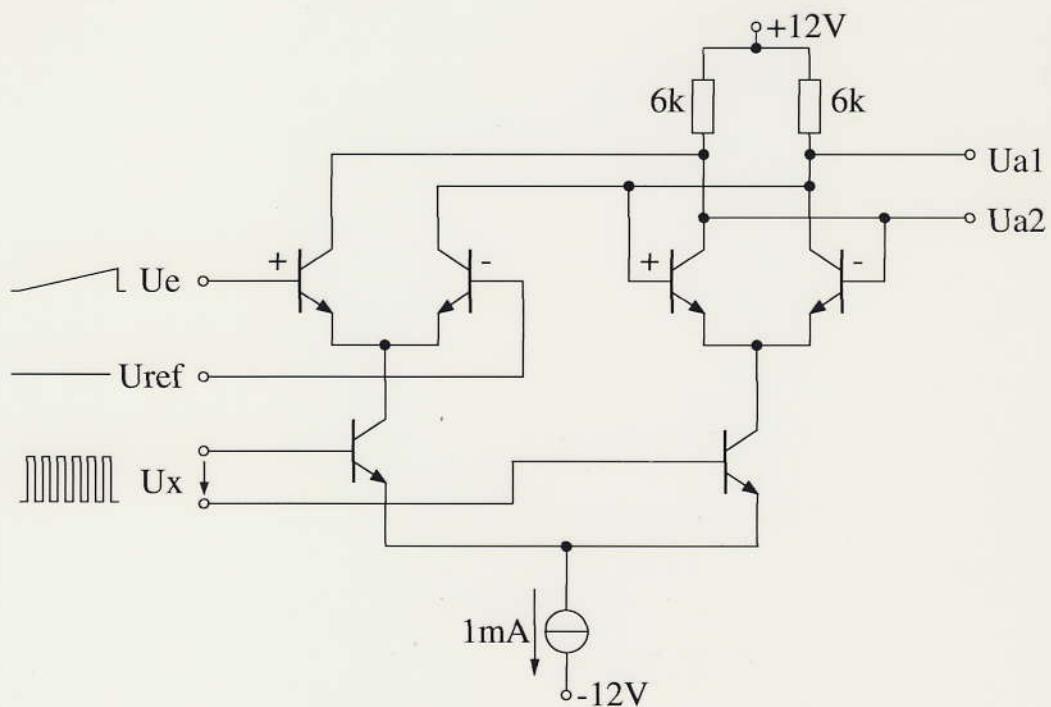
$$\begin{cases} \downarrow \\ g_m R \geq 1 \\ \rightarrow U_a \rightarrow \pm \infty \end{cases}$$

praktisch Begrenzung durch
Grobbaugleichschaltung

je gröber die $i_{in}(t)$ ist, um so schneller bewegt sich die Schaltung vom Gleichgewichtszustand weg

→ Komparator reagiert schneller für große Differenz ($U_e - U_{ref}$)

Fehl Trajektorie



High-speed dual-differential comparator/sense amp

NE521

TYPICAL PERFORMANCE CHARACTERISTICS

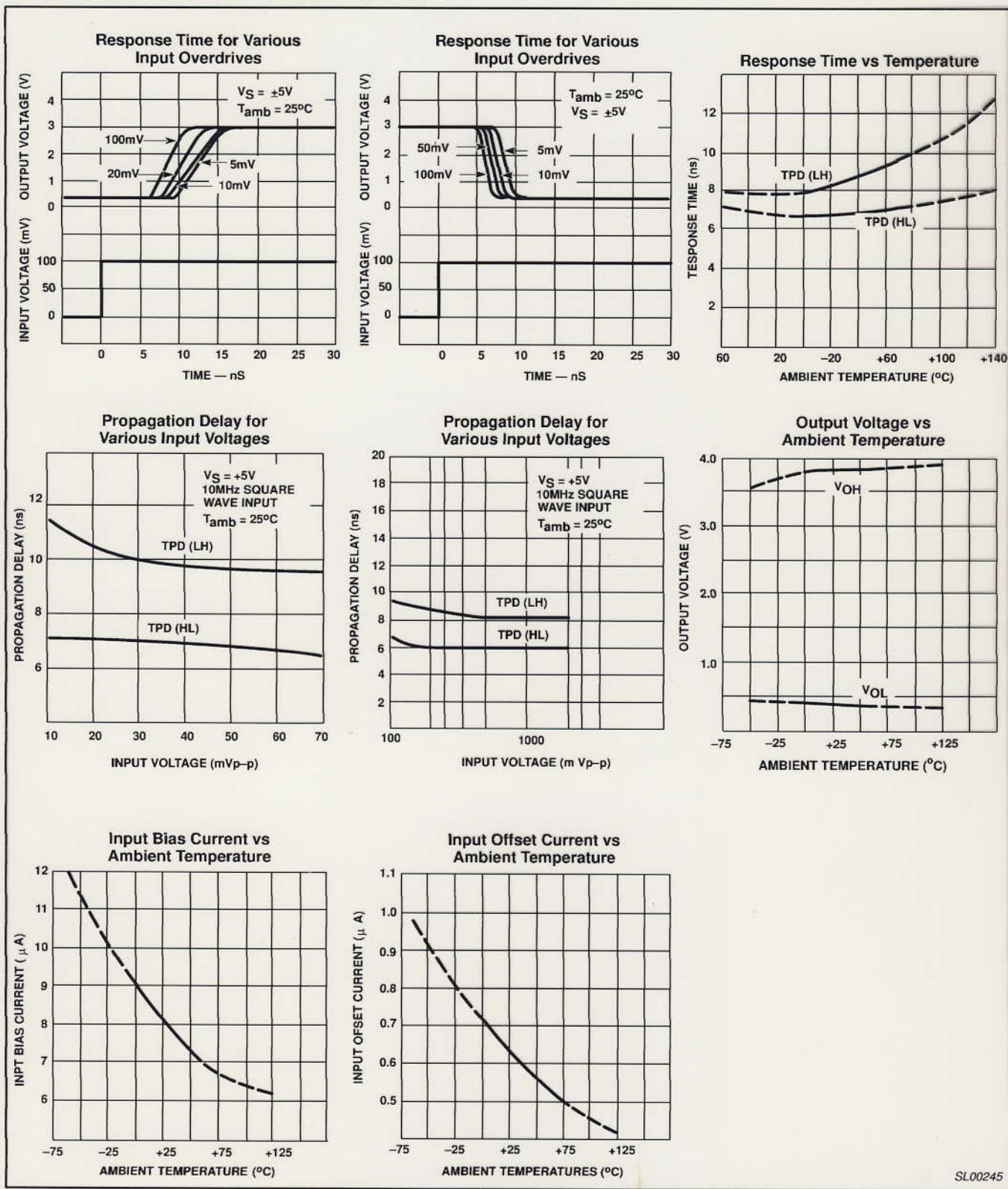


Figure 4. Typical Performance Characteristics

SL00245